	US ATLAS **PHASE II Upgrade** **BASIS of ESTIMATE (BoE)**	**Date of Est:** **11/21/2015** **Prepared by: H. Chen; J. Zhang** **Responsible Inst: ANL & BNL** **Docdb #:**
WBS number: 6.7.3	**WBS Title: TDAQ FELIX Development**	
WBS Dictionary Definition: This WBS covers the FELIX development and production test of FELIX boards for TDAQ Phase-II upgrade. This includes design and prototype testing of next generation of FELIX board for ATLAS TDAQ Phase-II upgrade. In production phase, a production test bench will be built and used to perform production QA/QC procedures on 20% (~$1M) of production FELIX boards.		
Estimate Type (check all that apply – see BOE Report for estimate type by activity): ___ Work Complete ___ Existing Purchase Order __x_ Catalog Listing or Industrial Construction Database ___ Documented Vendor Estimate based on Drawings/ Sketches/ Specifications __x_ Engineering Estimate based on Similar Items or Procedures __x_ Engineering Estimate based on Analysis __x_ Expert Opinion		
Supporting Documents (including but not limited to):		

Details of the Base Estimate (explanation of the Work)

The WBS scope covers development of next generation of FELIX board for ATLAS TDAQ Phase-II upgrade, from prototype design to final production test. The new FELIX board will be based on Xilinx Virtex/Kintex Ultrascale+ FPGA, have 24 transceiver links to interface to detector front end readout with lpGBTx transceivers, and PCI Express Gen4 x16 lane interface to DAQ PC mother board. The FELIX board can also be configured to have 48 transmitter links, to be used as a TTC distribution module to detector front end electronics.

For development of new FELIX board, the following tasks will be performed.

1. Design stage (FY18-FY20): early prototype design and evaluation test of new FELIX board. A lab test bench will be set up to evaluate the board, with focus on the basic hardware, firmware and software functionalities.
2. Prototype stage (FY21-FY22): prototype design of new FELIX board. Prototype FELIX board will be built and used to verify the system level performance. An integration test stand will be built to evaluate the board, with focus on the system integration to the detector front end readout, exercise hardware, firmware and software integration and data flow management.
3. Production stage (FY23): production test of new FELIX board. Total ~200 production FELIX boards will be produced and tested for Phase-II TDAQ upgrade. All production FELIX boards will go through production QA/QC procedures, only qualified FELIX boards will be shipped to CERN for installation and commissioning.

For new FELIX development, both ANL and BNL will work together to carry out the design, prototype and production phases. It is estimated that ~0.5 FTE is needed for FY18, ~2 FTE per year are needed from FY19-FY20, and ~2.5 FTEs per year are needed from FY21-FY22, and ~1.8 FTEs per year are needed for FY23.

Labor estimates are based on the past experience of the FELIX development and PCIe card development in Phase-I upgrade. The M&S costs cover prototype FELIX fabrication, preparation of FELIX test stands and lab test for FY18-FY21. For FY22-FY23, the M&S costs cover production FELIX fabrication and QA/QC procedures in the production test bench.

Travel in FY18-FY23 is needed for engineers travel to CERN, discuss the design of next generation of FELIX board and report progress and test results in collaboration meetings.

A cost summary is tabulated below and more details can be found in the comments section.

	Materials [$]	Travel [$]	Engineer [hr]	Tech [hr]	Labor [$]
Design	80,000	40,000	7992	0	1,023,452
Prototype	540,000	40,000	7104	1776	1,165,287
Production	500,000	20,000	2309	888	429,842

* off-project effort is supported by research funds.

Assumptions:

The costs are based on design and prototype cycles from FY18-FY22, and full production will take place in FY23, though M&S cost for production is spread in FY22 & FY23.

Risk Analysis

Schedule Risk: **Probability: Moderate, Impact: Low, Overall: Low**
Potential Problem: Late delivery of FPGAs and discovery of problems that can only be found at the bench test and system integration test may impact the project schedule.
Mitigation: Start board evaluation and system integration test early, at each prototype stage, perform detailed tests and apply rigorous performance standards at all times. Add engineering efforts where needed. Use schedule contingency.

Cost Risk: **Probability: Moderate, Impact: Low, Overall: Low**
Potential Problem: discovery of problems may require a new revision of the board design.
Mitigation: Add engineering efforts to perform extensive and comprehensive board evaluation test, aim to solve all potential issues in early prototype runs.

Technical/Scope Risk: **Probability: Moderate, Impact: Low, Overall: Low**
Potential Problem: Technical issues such as link stability, FPGA resources usage may only be discovered at the system integration test, and would most likely require revision of the board.
Mitigation: Start board evaluation and system integration test early, at each prototype stage, perform detailed tests and apply rigorous performance standards at all times. Add engineering efforts where needed.

M&S Contingency Rules Applied

Rule 5: 40%

Items with a detailed conceptual level of design; items adapted from existing designs but with extensive modifications, and/or made more than 2 years previous with documented costs.

Labor Contingency Rules Applied

Rule 5: 50%

While the principal nature of the task is understood and analogous to past activities (e.g. fabrication activity similar to, but not exactly like, items fabricated for other activities; design labor for items similar to, but not exactly like, previous designs), the stringent design requirement warrants a conservative labor contingency.

Comments:

Next generation of FELIX:

Development of next generation of FELIX board will go through design and prototype phases. Design specification will be carefully defined by FELIX collaborators, and a early prototype FELIX board will go through lab test to verify basic hardware, firmware and software functionalities. It will feed back to the next iteration of prototype design. Prototype FELIX will be used in the system integration test. An integration test stand will be built to evaluate the board, with focus on the system integration to the detector front end readout, exercise hardware, firmware and software integration and data flow management. This will provide important information before the final production FELIX board design is finalized, and test results will be used to prepare for the PRR of FELIX board. Production of FELIX boards will be shared by international FELIX collaborators, US will only produce ~20% (~200) FELIX boards. All FELIX boards will go through production QA/QC procedures, only qualified boards will be shipped to CERN for installation and commissioning

Labor and M&S

Labor hours are dominated by FELIX board design and evaluation test, including specification writing, board schematics and layout design, the design of test stand, software and firmware development in design and prototype phases of the FELIX boards. An integration test stand will be built to evaluate the system integration to the detector front end readout, exercise hardware, firmware and software integration and data flow management. During the production phase, the work is mostly debugging and measurements with test stand developed in the prototype phase.

In FY18-FY19, travel (approx. $10k/yr) is needed for engineers travel to CERN, discuss the specification of FELIX board. In FY20-FY23, travel (approx. $20k/yr) is needed for engineers travel to CERN, discuss the FELIX board design and report test results in collaboration meetings. In early years (FY18-FY19), M&S ($20k/year) costs cover test bench with evaluation board. For FY20-FY21, the M&S ($40k/year) costs cover prototype FELIX fabrication, preparation of FELIX test stands (workstation, equipment, electrical and mechanical materials and test board procurements) and lab test. For FY22-FY23, the M&S ($500k/year) costs cover production FELIX fabrication and QA/QC procedures in the production test bench.

Cost and schedule of the project are further illustrated by the following table:

DOE 6.7.3		**FELIX_ANL**											
			Total cost	-	69.689	244.613	254.398	262.029	269.890	212.095	-	-	1312.714
			Total FTE	0.00	0.25	1.00	1.00	1.00	1.00	0.80	0.00	0.00	5.05
			Designer	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
			Sr Engr	0.00	0.25	0.50	0.50	0.50	0.50	0.30	0.00	0.00	2.55
			Jr Engr	0.00	0.00	0.50	0.50	0.50	0.50	0.50	0.00	0.00	2.50
			Sr Tech	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
			Jr Tech	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
			Student	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
			Uncosted Physicist	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
		FELIX Hardware/Firmware											
	FLXA1000	Design											
			Total cost	-	69.689	244.613	254.398	-	-	-	-	-	568.699
			Total FTE	0.00	0.25	1.00	1.00	0.00					2.25
			Designer										0.00
			Sr Engr		0.25	0.50	0.50						1.25
			Jr Engr			0.50	0.50						1.00
			Sr Tech										0.00
			Jr Tech										0.00
			Student										0.00
			Uncosted Physicist										0.00
	FLXA1010	Prototype											
			Total cost	-	-	-	-	262.029	269.890	-	-	-	531.920
			Total FTE	0.00	0.00	0.00	0.00	1.00	1.00	0.00	0.00	0.00	2.00
			Designer										0.00
			Sr Engr					0.50	0.50				1.00
			Jr Engr					0.50	0.50				1.00
			Sr Tech										0.00
			Jr Tech										0.00
			Student										0.00
			Uncosted Physicist										0.00
	FLXA1020	Production											
			Total cost	-	-	-	-	-	-	212.095	-	-	212.095
			Total FTE	0.00	0.00	0.00	0.00	0.00	0.00	0.80	0.00	0.00	0.80
			Designer			-	-	-	-	-			0.00
			Sr Engr			-				*0.30*			0.30
			Jr Engr			-				*0.50*			0.50
			Sr Tech			-							0.00
			Jr Tech			-							0.00
			Student			-							0.00
			Uncosted Physicist			-							0.00
DOE 6.7.3		**FELIX_BNL**											
			Total cost	-	48.138	199.320	207.293	312.003	321.364	217.747	-	-	1305.866
			Total FTE	0.00	0.25	1.00	1.00	1.50	1.50	1.00	0.00	0.00	6.25
			Designer	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
			Sr Engr	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
			Jr Engr	0.00	0.25	1.00	1.00	1.00	1.00	0.50	0.00	0.00	4.75
			Sr Tech	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
			Jr Tech	0.00	0.00	0.00	0.00	0.50	0.50	0.50	0.00	0.00	1.50
			Student	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
			Uncosted Physicist	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
		FELIX Hardware/Firmware											
	FLXB1000	Design											
			Total cost	-	48.138	199.320	207.293	-	-	-	-	-	454.752
			Total FTE	0.00	0.25	1.00	1.00	0.00					2.25
			Designer										0.00
			Sr Engr										0.00
			Jr Engr		0.25	1.00	1.00						2.25
			Sr Tech										0.00
			Jr Tech										0.00
			Student										0.00
			Uncosted Physicist										0.00
	FLXB1010	Prototype											
			Total cost	-	-	-	-	312.003	321.364	-	-	-	633.367
			Total FTE	0.00	0.00	0.00	0.00	1.50	1.50	0.00	0.00	0.00	3.00
			Designer										0.00
			Sr Engr										0.00
			Jr Engr					1.00	1.00				2.00
			Sr Tech										0.00
			Jr Tech					0.50	0.50				1.00
			Student										0.00
			Uncosted Physicist										0.00
	FLXB1020	Production											
			Total cost	-	-	-	-	-	-	217.747	-	-	217.747
			Total FTE	0.00	0.00	0.00	0.00	0.00	0.00	1.00	0.00	0.00	1.00
			Designer			-	-	-	-	-			0.00
			Sr Engr			-							0.00
			Jr Engr			-				*0.50*			0.50
			Sr Tech			-							0.00
			Jr Tech			-				*0.50*			0.50
			Student			-							0.00
			Uncosted Physicist			-							0.00